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CLEARY, THOMAS J

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,880	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-18 recite the limitation "a predetermined finite set of signals." The term "predetermined" as used in the aforementioned claims is indefinite because it does not indicate a criteria to be used for predetermination, nor does it indicate a manner of implementing the predetermination. Therefore, the scope of the claimed invention for the aforementioned claims cannot be reasonably determined by one having ordinary skill in the art.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,488,688 to Gonzales et al. ("Gonzales").

5. In reference to Claim 1, Gonzales teaches a buffer having at least one trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), to observe and echo a predetermined finite set of signals transmitted on said bus, signals transmitted into said component and signals transmitted out of said component (See Column 2 Lines 23-26); wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus (See Figure 1 Number 22 and Column 2 Lines 55-59).

6. In reference to Claim 6, Gonzales teaches a buffer having at least one trigger (See Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 1 and Column 2 Lines 23-26), observing and echoing a predetermined finite set of signals transmitted on the bus, signals transmitted into a component and signals transmitted out of said component (See Column 2 Lines 23-26); wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus (See Figure 1 Number 22 and Column 2 Lines 55-59).

7. In reference to Claim 10, Gonzales inherently includes a memory and an I/O port. Gonzalez teaches a microprocessor (See Figure 1 Number 21); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 1 Number 22 and Column 2 Lines 55-59); and a buffer means, integrated on a component coupled to one of said busses (See Figure 1 and Column 2 Lines 23-26), for observing and echoing a predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Figure 1 and Column 2 Lines 23-26).

8. In reference to Claim 14, Gonzales inherently includes a memory and an I/O port. Gonzalez teaches a microprocessor (See Figure 1 Number 21); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 1 Number 22 and Column 2 Lines 55-59); and a buffer, having at least one trigger (See Column 2 Lines 23-26), integrated on a component coupled to one of said busses (See Figure 1 and Column 2 Lines 23-26), to observe and echo a predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Figure 1 and Column 2 Lines 23-26).

9. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,903,719 to Yamamoto ("Yamamoto").

10. In reference to Claim 1, Yamamoto teaches a buffer having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), to observe and echo a predetermined finite set of signals transmitted on said bus, signals transmitted into said component and signals transmitted out of said component (See Column 2 Lines 35-44); wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus (See Column 2 Lines 12-16).

11. In reference to Claim 6, Yamamoto teaches a buffer having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component connected with a bus (See Figure 2 and Column 2 Lines 3-5), observing and echoing a predetermined finite set of signals transmitted on the bus, signals transmitted into a component and signals transmitted out of said component (See Column 2 Lines 35-44); wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus (See Column 2 Lines 12-16).

12. In reference to Claim 10, Yamamoto teaches a memory (See Figure 2 Number 12); an I/O port (See Figure 2 Number 17); and a microprocessor (See Figure 2 Number 11); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 2 Number 13 and Column 2 Lines 12-16); and a buffer means, integrated on a component coupled to one of said busses (See Figure 2 and Column 2 Lines 3-5), for observing and echoing a

predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Column 2 Lines 35-44).

In reference to Claim 14, Yamamoto teaches a memory (See Figure 2 Number 12); an I/O port (See Figure 2 Number 17); and a microprocessor (See Figure 2 Number 11); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 2 Number 13 and Column 2 Lines 12-16); and a buffer, having at least one trigger (See Figure 2 Number 18 and Column 2 Lines 23-26), integrated on a component coupled to one of said busses (See Figure 2 and Column 2 Lines 3-5), to observe and echo a predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Column 2 Lines 35-44).

13. Claims 1, 6, 10, and 14 are rejected under 35 U.S.C. 102(a) as being anticipated by US Patent Number 6,119,254 to Assouad et al. ("Assouad").

14. In reference to Claim 1, Assouad teaches a buffer having at least one trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), to observe and echo a predetermined finite set of signals transmitted on said bus, signals transmitted into said component and signals transmitted out of said component (See Column 7 Lines 50-62); wherein said bus is one

of a memory bus, a data bus, an address bus, and a control bus (See Figure 3 Number 105).

15. In reference to Claim 6, Assouad teaches a buffer having at least one trigger (See Column 7 Lines 43-46), integrated on a component connected with a bus (See Figure 3 Numbers 104 and 105), observing and echoing a predetermined finite set of signals transmitted on the bus, signals transmitted into a component and signals transmitted out of said component (See Column 7 Lines 50-62); wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus (See Figure 3 Number 105).

16. In reference to Claim 10, Assouad teaches a memory (See Figure 3 Number 112); an I/O port (See Figure 3 Number 204); and a microprocessor (See Figure 3 Number 111); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 3 Numbers 105 and 209); and a buffer means, integrated on a component coupled to one of said busses (See Figure 3 Numbers 104 and 105), for observing and echoing a predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Column 7 Lines 50-62).

17. In reference to Claim 14, Assouad teaches a memory (See Figure 3 Number 112); an I/O port (See Figure 3 Number 204); and a microprocessor (See Figure 3

Number 111); wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus (See Figure 3 Numbers 105 and 209); and a buffer, having at least one trigger (See Column 7 Lines 43-46), integrated on a component coupled to one of said busses (See Figure 3 Numbers 104 and 105), to observe and echo a predetermined finite set of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of said component (See Column 7 Lines 50-62).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1, 2, 6, 7, 10, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,072,804 to Beyers, Jr. ("Beyers") in view of US Patent Number 5,933,594 to La Joie et al. ("La Joie") and knowledge which is well known in the art.

20. In reference to Claim 1, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are

transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a buffer having at least one trigger, coupled with one of a bus and a component connected with said bus, to observe and echo a predetermined finite set of signals transmitted on said bus; wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing signals by a monitoring system, which is equivalent to observing and echoing signals (See Column 2 Lines 34-41), from the external bus; and said bus being one of a data bus, and address bus, and a control bus (See Column 5 Lines 45-50). The signals monitored by LaJoie must inherently be determined prior to the system of LaJoie monitoring said signals. The signals monitored by LaJoie are inherently a finite set. The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 1, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

21. In reference to Claim 2, Beyers, La Joie, and knowledge commonly known in the art teach the limitations as applied to Claim 1 above. Beyers further teaches a bus,

which is equivalent to the observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 2, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

22. In reference to Claim 6, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a buffer having at least one trigger; observing and echoing a predetermined finite set of the signals transmitted on said bus, transmitted into the component, and transmitted out of the component; and wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing signals by a

monitoring system, which is equivalent to observing and echoing signals (See Column 2 Lines 34-41) from the external bus; and said bus being one of a data bus, and address bus, and a control bus (See Column 5 Lines 45-50). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 6, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

23. In reference to Claim 7, Beyers, La Joie, and knowledge commonly known in the art teach the limitations as applied to Claim 6 above. Beyers further teaches receiving the external signals (See Column 13 Lines 34-36); capturing the external signal (analogous to detecting the signal) (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer which is equivalent to reading the signal (See Column 14 Lines 4-5).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 1, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

24. In reference to Claim 10, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a memory; an I/O port; a microprocessor; wherein said memory, I/O port, and microprocessor are connected by a data bus, an address bus, and a control bus; and a buffer means, integrated on a component coupled to one of said busses, for observing and echoing a predetermined finite set of signals transmitted on a bus, signals transmitted into the component, and signals transmitted out of said component. La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer (See Figure 1 Number 20) that stores data captured from the external bus, which is equivalent to observing and echoing signals (See Column 14 Lines 1-13). La Joie teaches the processor (See Figure 1 Number 10) being connected by the processor bus to a control interface (See Figure 1 Number 24) which means the bus would necessarily include a control bus, and a memory (See Figure 1 Number 22) which means the bus would necessarily include a data bus and an address bus. La Joie further teaches that common components of busses include address lines, data lines, and control lines (See Column 5 Lines 45-46).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 10, in

order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

25. In reference to Claim 11, Beyers and La Joie teach the limitations as applied Claim 10 above. Beyers further teaches receiving the external signals (See Column 13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer (analogous to reading the signal (See Column 14 Lines 4-5).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 11, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

26. In reference to Claim 14, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a memory; an I/O port; a microprocessor; wherein said memory, I/O port, and microprocessor are connected by a data bus, an address bus, and a control bus; and a buffer means, integrated on a component coupled to one of said busses, for observing and echoing a predetermined finite set of signals transmitted on a bus, signals transmitted into the component, and signals transmitted out of said component. La Joie

teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer (See Figure 1 Number 20) that stores data captured from the external bus, which is equivalent to observing and echoing signals) (See Column 14 Lines 1-13). La Joie teaches the processor (See Figure 1 Number 10) being connected by the processor bus to a control interface (See Figure 1 Number 24) which means the bus would necessarily include a control bus, and a memory (See Figure 1 Number 22) which means the bus would necessarily include a data bus and an address bus. La Joie further teaches that common components of busses include address lines, data lines, and control lines (See Column 5 Lines 45-46).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the invention of Claim 14, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

27. In reference to Claim 15, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers further teaches a bus, which is equivalent to the observability bus, connected between a port on the analyzer buffer, which is equivalent to the observability port) (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control, which is equivalent to the logic analyzer and bus analyzer (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column

13 Lines 34-36); capturing the external signal, which is equivalent to detecting the signal (See Column 13 Lines 36-38); defining a data capture window, which is equivalent to accessing the signal (See Column 14 Lines 13-15); and storing the data in the analyzer buffer, which is equivalent to reading the signal (See Column 14 Lines 4-5).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the inventions of Claim 15, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

28. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 2 and 15 above, and further in view of US Patent Number 6,496,583 to Nakamura et al. ("Nakamura").

29. In reference to Claim 3, Beyers and La Joie teach the limitations as applied to Claim 2 above. Beyers and La Joie do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

One of ordinary skill in the art would combine the device of Beyers and La Joie with the device of Nakamura, resulting in the invention of Claim 3, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

30. In reference to Claim 16, Beyers and La Joie teach the limitations as applied to Claim 15 above. Beyers and La Joie do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

One of ordinary skill in the art would combine the device of Beyers and La Joie with the device of Nakamura, resulting in the invention of Claim 16, in order to provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

31. Claims 4, 8, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 1, 6, 10, and 14 above, and further in view of US Patent Number 6,147,863 to Moore et al. ("Moore").

32. In reference to Claim 4, Beyers and La Joie teach the limitations as applied to Claim 1 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Moore, resulting in the invention of

Claim 4, in order to allow the device to be compatible with a wide range of devices because PCI busses and ISA busses are standardized busses with widespread use.

33. In reference to Claim 8, Beyers and La Joie teach the limitations as applied to Claim 6 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Moore, resulting in the invention of Claim 8, in order to allow the device to be compatible with a wide range of devices because PCI busses and ISA busses are standardized busses with widespread use.

34. In reference to Claim 12, Beyers and La Joie teach the limitations as applied to Claim 10 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Moore, resulting in the invention of

Claim 12, in order to allow the device to be compatible with a wide range of devices because PCI busses and ISA busses are standardized busses with widespread use.

35. In reference to Claim 17, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Moore, resulting in the invention of Claim 17, in order to allow the device to be compatible with a wide range of devices because PCI busses and ISA busses are standardized busses with widespread use.

36. Claims 5, 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 1 and 6 above, and further in view of US Patent Number 6,587,679 to Hokao ("Hokao").

37. In reference to Claim 5, Beyers and La Joie teach the limitations as applied to Claim 1 above. Beyers and La Joie do not teach the buffer being configured to observe and echo signals transmitted by wireless communication. Hokao teaches a method of

monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Hokao, resulting in the invention of Claim 5 in order to monitor signals that are communicated wirelessly (See Column 1 Lines 33-38 of Hokao) as well as monitor the signal without affecting it or being detected by the communicating parties.

38. In reference to Claim 9, Beyers and La Joie teach the limitations as applied to Claim 6 above. Beyers and La Joie do not teach the signals being transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Hokao, resulting in the invention of Claim 9, in order to monitor signals that are communicated wirelessly (See Column 1 Lines 33-38 of Hokao) as well as monitor the signal without affecting it or being detected by the communicating parties.

39. In reference to Claim 13, Beyers and La Joie teach the limitations as applied to Claim 10 above. Beyers and La Joie do not teach the signals being transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Hokao, resulting in the invention of Claim 13, in order to monitor signals that are communicated wirelessly (See Column 1 Lines 33-38 of Hokao) as well as monitor the signal without affecting it or being detected by the communicating parties.

40. In reference to Claim 18, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers and La Joie do not teach the buffer being configured to observe and echo signals transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Hokao, resulting in the invention of Claim 14, in order to monitor signals that are communicated wirelessly (See Column 1 Lines 33-38 of Hokao) as well as monitor the signal without affecting it or being detected by the communicating parties.

Specification

41. The disclosure is objected to because of the following informalities: the title of the invention appears to improperly use the word "observer". The Examiner recommends

changing the title to "ON-CHIP OBSERVABILITY BUFFER TO OBSERVE BUS TRAFFIC".

Appropriate correction is required.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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